Code.No: 07A40401 | R07 | SET-1

II B.TECH – II SEM EXAMINATIONS, DECEMBER - 2010
DIGITAL IC APPLICATIONS
(ELECTRONICS AND INSTRUMENTATION ENGINEERING)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks

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1.a) Design CMOS transistor circuit for 2-input OR gate. With the help of function table explain the circuit.
b) Design a CMOS transistor circuit that has the functional behavior

f (Z) = $\overline{A.\overline{(B+C)}}$ [8+8]

2.a) Design TTL three state NAND gate and explain the operation with the help of functional table.
b) Explain how CMOS TTL interfacing can be achieved. Give the input and output levels of voltages. [8+8]

3.a) Explain the difference between function and procedure supported by VHDL. Give the necessary examples.
b) Explain the various data types supported by VHDL. Give the necessary examples. [8+8]

4. Explain with an example the syntax and the function of the following VHDL statements.
a) Variable assignment statements
b) Next statements
c) Assertion statements
d) Report statements [4+4+4+4]

5. Design a two-digit BCD adder with logic gates. Using this logic write the VHDL Program in behavioral structural style of modeling. [16]

6 Design a 8×8 combinational multiplier and write the necessary VHDL program in structural model. [16]

7.a) Differentiate between Asynchronous counter and synchronous counter? Design a 4-bit counter in both modes and estimate the propagation delay.
b) Design a modulo -100 counter using 74×163 ICs. [8+8]

8.a) Discuss how PROM, EPROM and EEPROM technologies differ from each other.
b) With the help of timing waveforms, explain read and write operations of DRAM. [8+8]

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DIGITAL IC APPLICATIONS
(ELECTRONICS AND INSTRUMENTATION ENGINEERING)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks

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1.a) Design a CMOS transistor circuit that has the functional behavior $f(Z) = \overline{(\overline{A+B})(\overline{A+D})(\overline{B+D})}$

b) Distinguish between static and dynamic power dissipation of CMOS circuit. Derive the expression for dynamic power dissipation. [8+8]

2.a) Design 2-input LS-TTL NAND gate and explain its operation. Give the function table, truth table.

b) Compare CMOS, TTL and ECL with reference to logic levels, DC noise margin, propagation delay and fan-out. [8+8]

3.a) Explain the difference between VHDL program structure and other procedural language program structure.

b) Write a VHDL program to detect prime number of a 8-bit input. [8+8]

4.a) Design an excess-3 decimal counter using 74*163 and explain the operation with help of timing waveforms.

b) Design an 8-bit synchronous binary counter with serial enable control. [8+8]

5.a) Design an 8-bit parallel-in and serial-out shift register. Explain the operation of the shift register with the help of timing diagram

b) Difference between serial adder and parallel adder. [8+8]

6.a) Design sequence detector to detect the 1101 sequence using JK flip flops.

b) Design divide by 6-counter using T-flip flop. Write state table and reduce the expression using K-map. [8+8]

7.a) Give the comparison between PROM, PLA and PAL.

b) Explain how a 4×4 binary multiplier can be designed using 256×8 ROM. [8+8]

8. Explain the following terms with reference to CMOS logic.
a) Logic Levels.
b) Noise margin.
c) Transition time
d) Propagation delay [4+4+4+4]

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Code.No: 07A40401 | R07 | SET-3

II B.TECH – II SEM EXAMINATIONS, DECEMBER - 2010
DIGITAL IC APPLICATIONS
(ELECTRONICS AND INSTRUMENTATION ENGINEERING)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
All questions carry equal marks

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1.a) Explain the concept of sinking and sourcing currents. How are they estimated for CMOS families?
b) Design CMOS transistor circuit for 4-input OR-AND inverter gate. With the help of function table explain the circuit. [8+8]

2.a) Design 2-input LS-TTL NOR gate and explain its operation. Give the function table, truth table.
b) Explain the behavioral difference between simple transistor logic inverter and schottkey logic inverter. [8+8]

3.a) Explain the time dimension and simulation in VHDL. Give the necessary examples.
b) Explain the difference between variable data type and signal data types. Give the necessary examples. [8+8]

4. Design the logic circuit and write a data-flow style VHDL program for the following functions
a) F(X) = $\sum$ A BCD (0, 1, 2, 5, 7, 8, 10, 14, 15) + d (3, 6, 11)
b) F(Y) = π A BC D (1, 4, 5, 7, 9, 11, 12, 13, 15) [8+8]

5.a) Design 8-bit ALU circuit using two 74LS181 ICs.
b) Design a 3-input 5-bit multiplexer. Write the truth table and draw the logic diagram and write VHDL program in dataflow model. [8+8]

6.a). Design a divide by 96-counter using 7490 ICs.
b) i) How many flip flops are required to build a binary counter that count from 0 to 1024?
ii) Determine the frequency at the output of last (MSB) flip flop for an input clock frequency of 2MHz.
iii) If the counter is initially at zero, what count it will hold after 2060clock pulses?
iv) Draw the block diagram for the above counter using TTL integrated circuit. [8+8]

7.a) How many ROM bits are required to build a 16-bit adder/ substractor with mode control, carry input, carry output and two complement overflow output? Show the block schematic with all inputs and outputs.
b) Design an 8*4 diode ROM using 74X138 for the following data starting from the location 1, 4, 9, B, A, O, F, C. [8+8]

8.a) Compare HC,HCT,VHC, and VHCT CMOS logic families with the help of output specifications with Vcc from 4.5 to 5.5V.

b) Explain the following terms.
i) Sequential Statement.
ii) Concurrent Statement. [8+4+4]

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(ELECTRONICS AND INSTRUMENTATION ENGINEERING)

Time: 3hours **Max.Marks:80**

Answer any FIVE questions
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1.a) Explain the circuit diagram of basic CMOS gate and explain its operation.
b) Explain the electrical characteristics of CMOS of
i) CMOS steady state electrical behavior.
ii) CMOS dynamic state electrical behavior. [6+10]

2.a) Draw and explain the operation of transistor inverter with its transfer characteristics.
b) What are the characteristics of TTL families? [10+6]

3.a) Explain the differences between variable data type and signal data types. Give the necessary examples.
b) Design and explain 16×1 multiplexer and Write a VHDL program in data flow model. [8+8]

4. Explain with an example the syntax and the function of the following VHDL statements.
a) Variable assignment statements
b) Next statements
c) Assertion statements
d) Report statements [4+4+4+4]

5.a) Distinguish between latch and flip-flop. Show the logic diagram for both. Explain the operation with the help of function table
b) Design a Modulo-12 ripple counter using 74×74? Write a VHDL program for this logic using data flow style. [8+8]

6. Write VHDL program for 8-bit comparator circuit. Using this entity write VHDL program for 24-bit comparator. Show the additional logic used for this purpose use structural style or modeling. [16]

7.a) Write a behavioral VHDL program to compare 16-bit signed and unsigned integers.
b) Difference between PROM, EPROM, PAL, PLA. [8+8]

8.a) Draw the basic cell structure of Dynamic RAM. What is the necessity of refresh cycle Explain the necessity of two-dimensional decoding mechanism in memories.
b) Draw MOS transistor memory cell in ROM and explain the operation. Explain the timing requirements of refresh operation. [8+8]

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